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JC930 U.S. PTO 09/28/00

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PTO/SB/05 (12/97)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 42390.P9239 Total Pages 3

First Named Inventor or Application Identifier Rajendran Nair

Express Mail Label No. EL 234 217 506 US

JC836 U.S. PTO 09/677698 09/28/00

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 18)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 7)

4. X Oath or Declaration (Total Pages 5)
   a. X Newly Executed (Original or Copy)
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. ______ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. X Assignment Papers (cover sheet & documents(s))

9. ____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
X b. Power of Attorney (Executed)

10. ____ English Translation Document (if applicable)

11. ____ a. Information Disclosure Statement (IDS)/PTO-1449
____ b. Copies of IDS Citations

12. ____ Preliminary Amendment

13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)

14. ____ a. Small Entity Statement(s)
____ b. Statement filed in prior application, Status still proper and desired

15. ____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. X Other: Attorney signature page including Copy of postcard and Certificate of Express Mailing pursuant to CFR §1.10.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
____ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No:____________________

18. **Correspondence Address**
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or
X Correspondence Address Below

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FEE TRANSMITTAL FOR FY 2000

TOTAL AMOUNT OF PAYMENT ($) $ 730.00

Complete if Known:
Application No. Not Yet Assigned
Filing Date September 28, 2000 (concurrently herewith
First Named Inventor Rajendran Nair
Group Art Unit Not Yet Assigned
Examiner Name Not Yet Assigned
Attorney Docket No. 42390.P9239

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

Deposit Account Number 02-2666
Deposit Account Name ______

[ ] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

2. X **Payment Enclosed:**
X **Check**
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FEE CALCULATION

1. **BASIC FILING FEE**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility application filing fee	690.00
106	310	206	155	Design application filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 690.00

2. **EXTRA CLAIM FEES**

			Extra Claims		Fee from below		Fee Paid
Total Claims	19	– 20** =	0	X	18.00	=	
Independent Claims	3	– 3** =	0	X	78.00	=	
Multiple Dependent						=	

****Or number previously paid, if greater; For Reissues, see below.**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 0.00

Patent fees are subject to annual revisions. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid.
See Forms PTO/SB/09-12

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,210	241	605	Petition to revive unintentionally abandoned application	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	690	246	345	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	690	249	345	For each additional invention to be examined (see 37 CFR 1.129(a))	

Other fee (specify) ____________________ ______

Other fee (specify) ____________________ ______

SUBTOTAL (3) $ 40.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Dennis A. Nicholls

Signature Dennis A. Nicholls **Date** 28 Sept., 2000

Reg. Number 42,036 **Deposit Account User ID** ____________ (complete if applicable)

Patent

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR WEAK INVERSION MODE MOS DECOUPLING CAPACITOR

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ATTORNEY'S DOCKET NO. 42390.P9239

Express Mail Certificate

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Tina Domingo
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T. Domingo
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9-28-2000
(Date signed)

METHOD AND APPARATUS FOR WEAK INVERSION MODE MOS DECOUPLING CAPACITOR

FIELD OF THE INVENTION

The present invention relates to a decoupling capacitor for an integrated circuit, and, more specifically, to a weak inversion capacitor for an integrated circuit.

BACKGROUND

Rapidly changing supply currents in digital circuits may induce noise onto the power supply lines and cause other problems. One technique to avoid this induced noise is to place capacitors, connected between the power supply traces and ground, physically near to those elements within the digital circuits that may require rapidly changing supply currents. Capacitors used in this manner are called decoupling capacitors or bypass capacitors. These are used in circuit designs as a means of supplying a low-impedance source of current when rapidly changing supply current is demanded by other elements of the circuit. Another viewpoint of decoupling capacitors is that they filter noise on the power supply lines.

Designers have various options when using decoupling capacitors on printed wiring boards. A mixture of high-capacitance electrolytic capacitors to suppress low-frequency changes and small-capacitance mica or ceramic capacitors to suppress high-frequency changes is commonly used. However, when placing decoupling capacitors on an

integrated circuit, the capacitors, as with other circuit elements such as the resistors, must be fabricated from silicon, doped silicon, and deposited metal.

One common method uses the gate capacitance inherent in a metal-oxide-semiconductor (MOS) transistor as the decoupling capacitor. For example, a standard enhancement-mode p-type MOS (PMOS) device, well-known in the art, may be used. In one configuration, the gate electrode is connected to the negative Vss connections and the drain, source, and substrate electrodes are connected to the positive Vcc connections. This configuration, called a "strong inversion" mode, was successfully used in integrated circuits until quite recently. Then, as gate oxide layers became thinner, the leakage current through the gate oxide became substantial. In another configuration, the drain, source, and substrate electrodes are connected to the negative Vss connections and the gate electrode is connected to the positive Vcc connections. This configuration, called a "depletion" mode, avoids the leakage through the gate oxide but has poor capacitance to voltage characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Figure 1 is a cross-sectional view of a poly-silicon-gate p-channel metal-oxide-semiconductor (PMOS) transistor.

Figure 2 is a schematic diagram of the PMOS transistor of Figure 1 configured as a strong inversion capacitor.

Figure 3 is a schematic diagram of the PMOS transistor of Figure 1 configured as a depletion mode capacitor.

Figure 4 is capacitance-to-voltage chart for the capacitors of Figures 2 and 3.

Figure 5 is a cross-sectional view of a platinum-silicide-gate PMOS transistor, according to one embodiment of the present invention.

Figure 6 is a schematic diagram of the PMOS transistor of Figure 5 configured as a weak inversion capacitor, according to one embodiment of the present invention.

Figure 7 is a capacitance-to-voltage chart for the capacitor of Figure 6, according to one embodiment of the present invention.

Figure 8 is an enlargement of a portion of the chart of Figure 7, according to one embodiment of the present invention.

DETAILED DESCRIPTION

A method and apparatus for providing a weak inversion mode metal-oxide-semiconductor (MOS) decoupling capacitor is described. In one embodiment, an enhancement-mode p-channel MOS (PMOS) transistor is constructed with a gate material whose work function differs from that commonly used. In one exemplary embodiment, platinum silicate (PtSi) is used. In alternate embodiments, the threshold voltage of the PMOS transistor may be changed by modifying the dopant levels of the substrate. In either embodiment the flat band magnitude of the transistor is shifted by the change in materials used to construct the transistor. When such a transistor is connected with the gate lead connected to the positive supply voltage and the other leads connected to the negative (ground) supply voltage, an improved decoupling capacitor results.

Referring now to Figure 1, a cross-sectional view of a poly-silicon-gate p-channel metal-oxide-semiconductor (PMOS) transistor 100 is shown. An n-type substrate 102 forms the basis of the transistor 100. A source area 104 and a drain area 106 are fabricated by diffusion to form highly-doped p-type (p+) material. A channel area 108 retains the n-type material of the substrate 102. A gate insulator area 112 is formed over the channel area 108. A gate region 110 is deposited over gate insulator area 112. In one common embodiment, gate region 110 is formed from highly-doped p-type (p+) polycrystalline silicon (poly-Si). The transistor 100 is finished with silicon oxide insulator layer 130

being deposited, and then etched, prior to the depositing of the source electrode 120, the gate electrode 122, and the drain electrode 124.

Referring now to Figure 2, a schematic diagram of the PMOS transistor 100 of Figure 1 configured as a strong inversion capacitor 200 is shown. In the Figure 2 embodiment, the gate electrode 208 is connected to the negative power supply line (Vss or ground). The drain electrode 202, the substrate electrode 204, and the source electrode 206 are connected together and to the positive power supply line (Vcc).

The Figure 2 configuration gives good capacitance values for use as a decoupling capacitor. However, as gate insulator area 112 becomes thinner in newer device processes, there may be a significant probability of direct band-to-band tunneling between the gate region 110 and the channel area 108. This would result in significant leakage current. When many of these decoupling capacitors are used on an integrated circuit, the leakage current through them may become significant.

Referring now to Figure 3, a schematic diagram of the PMOS transistor 100 of Figure 1 configured as a depletion mode capacitor 300 is shown. In the Figure 3 embodiment, the gate electrode 308 is connected to the positive power supply line (Vcc). The drain electrode 302, the substrate electrode 304, and the source electrode 306 are connected together and to the negative power supply line (Vss or ground).

The Figure 3 configuration was proposed to mitigate the leakage current discussed above in relation to the Figure 2 strong inversion

capacitor 200. When PMOS transistor 100 is configured as shown in Figure 3, it is in depletion mode, and therefore there is little mobile charge in channel area 108 which could tunnel through gate insulator area 112. Testing has shown the reduction in gate leakage current of depletion mode capacitor 300 is on the order of 10 to 100 times when compared with a strong inversion capacitor 200 of similar size.

Referring now to Figure 4, a capacitance-to-voltage chart for the capacitors of Figures 2 and 3 is shown. The Figure 4 chart shows normalized capacitance (C) on the y-axis. This assigns a base unit of capacitance per unit area to the Figure 2 decoupling capacitor. The x-axis shows voltage (V) where V is measured from the substrate to the gate ($V = V_{substrate} - V_{gate}$). Hence, V is a positive quantity for the Figure 2 decoupling capacitor, whereas V is a negative quantity for the Figure 3 decoupling capacitor.

Point 420 on the chart shows the performance of the Figure 2 decoupling capacitor. The capacitance of the strong inversion capacitor 200 is seen to be close to the maximum value of C for any point on the graph. Another way of viewing this is that the rate of change C/V is very low. The capacitance of strong inversion capacitor 200 stays essentially constant over a range of V from about 0.5 volts to above 2 volts. When used with a power supply voltage of 1.3 volts, the capacitance of strong inversion capacitor 200 is essentially constant in the noise range of interest around 1.3 volts.

Point 410 on the chart shows the performance of the Figure 3 decoupling capacitor. The capacitance of the depletion mode capacitor

300 is seen to be somewhat less (about 80%) in comparison to that of strong inversion capacitor 200, when both are used with a power supply voltage of 1.3 volts. A greater source of trouble is that when noise spikes pull down the local power supply voltage below 1.3 volts, the capacitance value goes down steeply.

Both of these potential problems with the depletion mode capacitor 300 may be partially mitigated by making the physical size of depletion mode capacitor 300 about twice the size of a comparable strong inversion capacitor 200. Since the depletion mode capacitor 300 has reduction in gate leakage current on the order of 10 to 100 times when compared to a similarly-sized strong inversion capacitor 200, a depletion mode capacitor 300 with twice the area of a strong inversion capacitor 200 will still have a reduction in gate leakage current on the order of 5 to 50 times. However, doubling the size of the decoupling capacitors may be a less than optimal solution.

Referring now to Figure 5, a cross-sectional view of a platinum-silicide (PtSi) gate PMOS transistor 500 is shown, according to one embodiment of the present invention. An n-type substrate 502 forms the basis of the transistor 500. A source area 504 and a drain area 506 are fabricated by diffusion to form highly-doped p-type (p+) material. A channel area 508 retains the n-type material of the substrate 502. A gate insulator area 512 is formed over the channel area 508. A gate region 510 is deposited over gate insulator area 512. Unlike the PMOS transistor 100 of Figure 1, in one embodiment of PMOS transistor 500 the gate region 510 is formed from highly-doped p-type (p+) platinum-

silicide (PtSi). In alternate embodiment, when decoupling differing supply voltages, gate region 510 may be formed from tantalum nitrate (TaN), iridium (Ir), nickel (Ni), arsenic (As), or other similar materials used either by themselves or as dopants of another material. The PMOS transistor 500 is finished with silicon oxide insulator layer 530 being deposited, and then etched, prior to the depositing of the source electrode 520, the gate electrode 522, and the drain electrode 524. Referring now to Figure 6, a schematic diagram of the PMOS transistor 500 of Figure 5 configured as a weak inversion capacitor 600 is shown, according to one embodiment of the present invention. In the Figure 6 embodiment, the gate electrode 608 is connected to the positive power supply line (Vcc). The drain electrode 602, the substrate electrode 604, and the source electrode 606 are connected together and to the negative power supply line (Vss or ground). The weak inversion capacitor 600 of Figure 6 differs principally from depletion mode capacitor 300 of Figure 3 in that the threshold voltage Vt of PMOS transistor 500 has been shifted by shifting the flat band of PMOS transistor 500. The expression "flat band" may be defined to mean that region where the work function difference between the gate and the body material that needs to be overcome so that the potential from the gate to the body of the device is flat.

In one embodiment of the present invention, the weak inversion capacitor 600 may be used as a decoupling or bypass capacitor for a power supply line. In alternate embodiments, however, weak inversion

capacitor 600 may also be used to decouple other sources of constant voltage, such as a precision voltage reference.

Referring now to Figure 7, a capacitance-to-voltage chart for the weak inversion capacitor 600 of Figure 6 is shown, according to one embodiment of the present invention. As with the Figure 4 chart, the Figure 7 chart shows normalized capacitance (C) on the y-axis. However, the x-axis shows voltage (V) where the Figure 7 V is measured from the gate to the substrate ($V = V_{gate} - V_{substrate}$). For this reason the chart of Figure 7 appears reversed about the y-axis when compared to the chart of figure 4.

Curve 710 duplicates the Figure 4 curve of depletion mode capacitor 300. For a situation where, for example, a power supply voltage Vcc of 0.4 volts is used, a decoupling capacitor such as depletion mode capacitor 300 has certain shortcomings. Curve 710 shows a low capacitance value for depletion mode capacitor 300 when at point 712, corresponding to a voltage-lowering noise spike, just when the maximum capacitance would be useful. A higher capacitance value for depletion mode capacitor 300 is obtained at point 714, when at full power supply voltage. Thus the depletion mode capacitor 300 exhibits the poor combination of low capacitance when noise exists and maximum leakage current at steady-state power conditions. It would be better to have a greater value of capacitance at 0.4 volts which would then increase, not decrease, with noise voltage.

In one embodiment of the present invention, the curve 710 is shifted to the right as shown by arrow 722 to form curve 720. This shift

may occur in response to changing the flat band magnitude from about 1.5 volts (point 716 on curve 710) to about 1.98 volts (point 762 on curve 720). Here the term "flat band magnitude" may have the definition of the size of the work function difference between the gate and the body material that needs to be overcome so that the potential from the gate to the body of the device is flat.

Curve 720 may represent the capacitance-to-voltage characteristics of a weak inversion capacitor 600. At the nominal supply voltage Vcc of 0.4 volts, at point 750, the capacitance value is low, but so is the leakage current value. At a point 760 corresponding to a voltage-lowering noise spike, the value of the capacitance shown in curve 720 is increasing rapidly with the size of the noise spike. By shifting the location of the flat band by about 0.48 volts, the curve 710 is shifted by about 0.48 volts to the right to form curve 720. This places the weak inversion portion of curve 720 within the range of interest 740 of a Vcc of 0.4 volts with 0.1 volts noise amplitude. At the nominal Vcc voltage of 0.4 volts, at point 750 on curve 720, a much larger value of capacitance C is observed. At a point 760 on curve 720, corresponding to a 0.1 volt noise spike, the value of capacitance C increases over that at point 750.

In one embodiment of the present invention, the shifting of the location of the flat band by about 0.48 volts may be accomplished by the use of the PMOS transistor 500 of Figure 5. In order to move the flat band magnitude from about 1.5 volts to about 1.98 volts, a change of about 0.48 volts, one embodiment changes the threshold voltage Vt

by changing the work function of the material comprising the gate area 510. The p+ poly-silicon gate area 110, which has a work function of approximately – 0.56 volts, is replaced by a p+ platinum-silicide gate area 510, which has a work function of approximately – 1.04 volts.

In alternate embodiments, other gate materials such as tantalum nitrate (TaN), iridium (Ir), nickel (Ni), or arsenic (As) may be used to obtain different flat band voltages, depending upon the magnitude of the voltage to be decoupled. These materials may be used by themselves or as dopants in silicon, poly-silicon, or other materials. In further embodiments, the flat band magnitude may be changed by changing the dopant levels of substrate 502 and channel area 508. Finally, in alternate embodiments when Vcc differs from 0.4 volts, a corresponding shift in flat band magnitude may be obtained by replacing the gate area 510 material or by changing the dopant levels in the substrate 502 and channel area 508.

Referring now to Figure 8, an enlargement of a portion 740 of the chart of Figure 7 is shown, according to one embodiment of the present invention. Curve 802 is a segment of curve 720 of Figure 7, and curve 804 is a segment of curve 710 of Figure 7. At point X 820 on curve 802, the value of V is that of the nominal Vcc, 0.4 volts. The initial capacitance of the weak inversion capacitor 600, at point X 820, is about 40% of that of a similar strong inversion capacitor 200. Therefore the area of weak inversion capacitor 600 would be increased by a factor of about 2.5 for equal capacitance of a strong inversion capacitor 200. The weak inversion capacitor 600 has a reduction in leakage of about 5

to 10 times when compared with the strong inversion capacitor 200, and, moreover, the leakage increases with inversion density in channel area 508. In practice this means that the leakage and the capacitance increases under conditions of noise (point Y 810), where the additional leakage is acceptable in exchange for the increased capacitance. The leakage is minimized at the steady state value of Vcc at point X 820.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

a metal-oxide-semiconductor transistor with a shifted flat band magnitude;

a gate electrode coupled to said metal-oxide-semiconductor transistor and to a positive voltage source; and

a source electrode, a drain electrode, and a substrate electrode coupled to each other and to a negative voltage source.

2. The apparatus of claim 1, wherein said metal-oxide-semiconductor includes a gate area material with a work function less than – 0.56 volts.

3. The apparatus of claim 2, wherein said gate area material is platinum silicate.

4. The apparatus of claim 2, wherein said gate area material is selected from the group consisting of tantalum nitrate, iridium, nickel, and arsenic.

5. The apparatus of claim 1, wherein said metal-oxide-semiconductor transistor includes a heavily-doped substrate area.

6. The apparatus of claim 1, wherein said metal-oxide-semiconductor transistor is a p-channel device.

7. The apparatus of claim 1, wherein said metal-oxide-transistor is an n-channel device.

8. A method, comprising:

shifting a flat band magnitude in a metal-oxide-semiconductor transistor;

coupling a gate electrode of said metal-oxide-semiconductor transistor to a positive voltage source; and

coupling a source electrode, a drain electrode, and a substrate electrode of said metal-oxide-semiconductor transistor to a negative voltage source.

9. The method of claim 8, wherein said shifting includes utilizing a gate area with a material whose work function is less than – 0.56 volts.

10. The method of claim 9, wherein said material is platinum silicate.

11. The method of claim 9, wherein said material is selected from the group consisting of tantalum nitrate, iridium, nickel, and arsenic.

12. The method of claim 8, wherein said shifting includes utilizing a substrate which is heavily-doped.

13. The method of claim 8, wherein said metal-oxide-semiconductor transistor is a p-channel device.

14. The method of claim 8, wherein said metal-oxide-semiconductor transistor is an n-channel device.

15. An apparatus, comprising:

means for shifting a flat band magnitude in a metal-oxide-semiconductor transistor;

means for coupling a gate electrode of said metal-oxide-semiconductor transistor to a positive voltage source; and

means for coupling a source electrode, a drain electrode, and a substrate electrode of said metal-oxide-semiconductor transistor to a negative voltage source.

16. The apparatus of claim 15, wherein said means for shifting includes a gate area with a material whose work function is less than – 0.56 volts.

17. The apparatus of claim 16, wherein said material is platinum silicate.

18. The apparatus of claim 16, wherein said material is selected from the group consisting of tantalum nitrate, iridium, nickel, and arsenic.

19. The apparatus of claim 15, wherein said means for shifting includes a substrate which is heavily-doped.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for providing a weak inversion mode metal-oxide-semiconductor (MOS) decoupling capacitor is described. In one embodiment, an enhancement-mode p-channel MOS (PMOS) transistor is constructed with a gate material whose work function differs from that commonly used. In one exemplary embodiment, platinum silicate (PtSi) is used. In alternate embodiments, the threshold voltage of the PMOS transistor may be changed by modifying the dopant levels of the substrate. In either embodiment the flat band magnitude of the transistor is shifted by the change in materials used to construct the transistor. When such a transistor is connected with the gate lead connected to the positive supply voltage and the other leads connected to the negative (ground) supply voltage, an improved decoupling capacitor results.

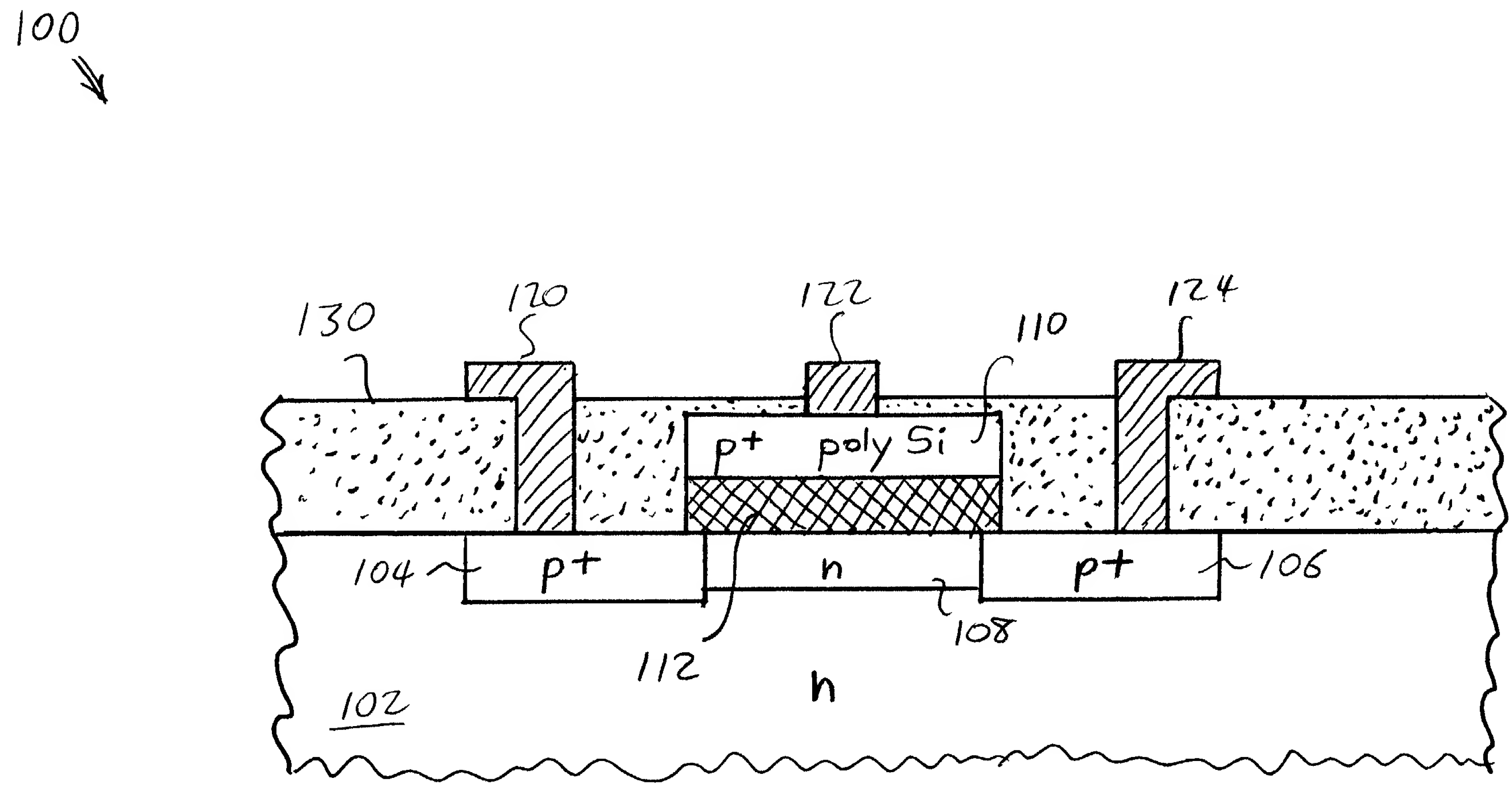


FIG. 1

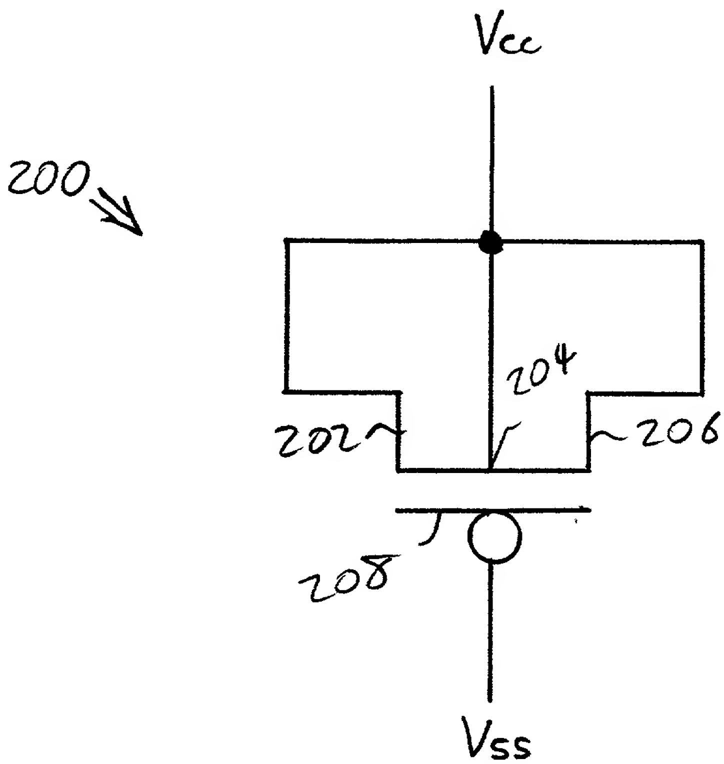


FIG. 2

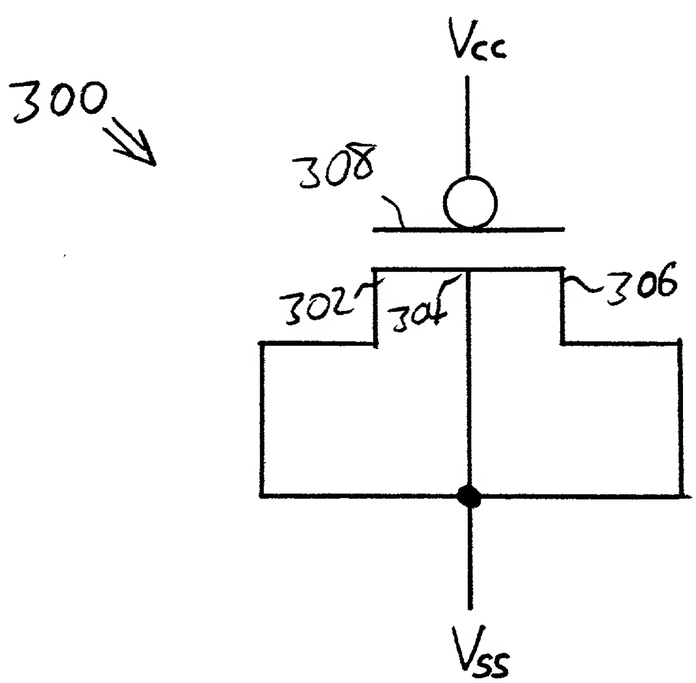


FIG. 3

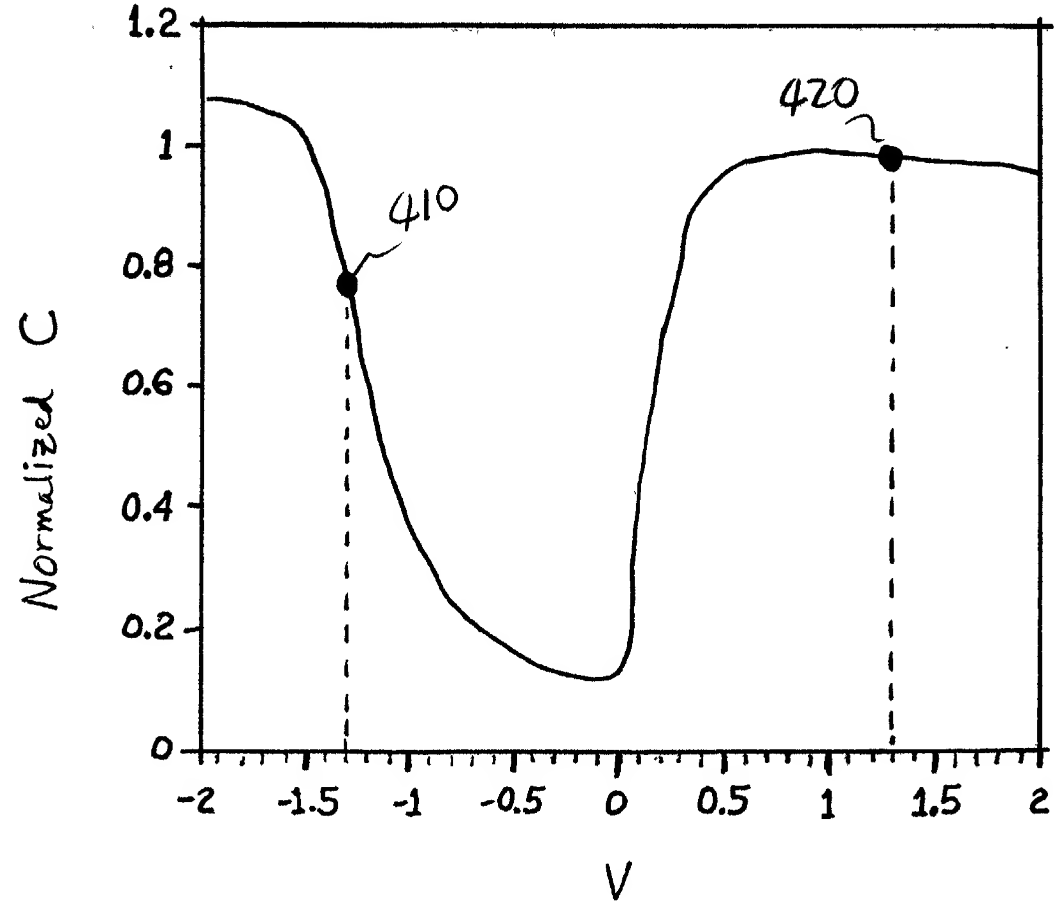


FIG.4

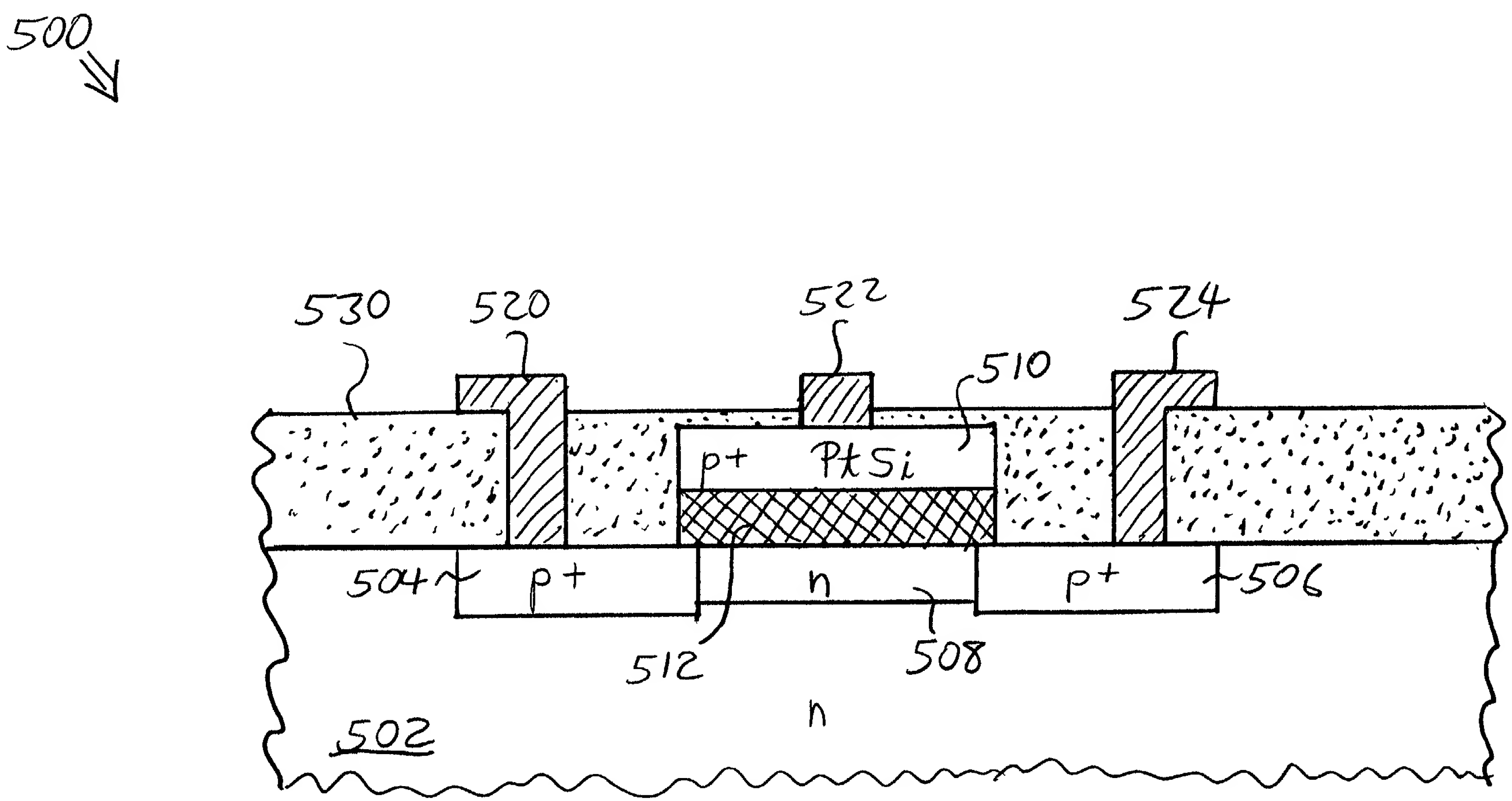


FIG. 5

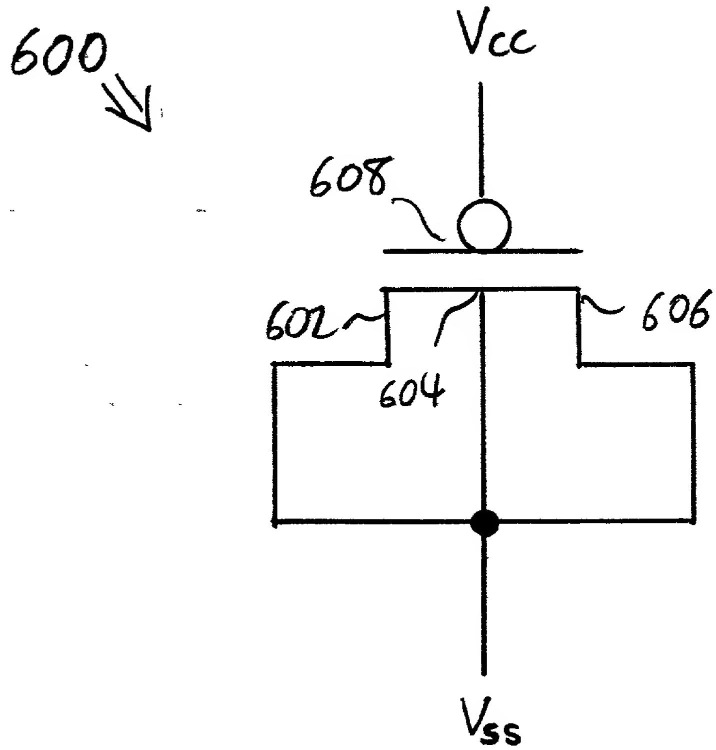
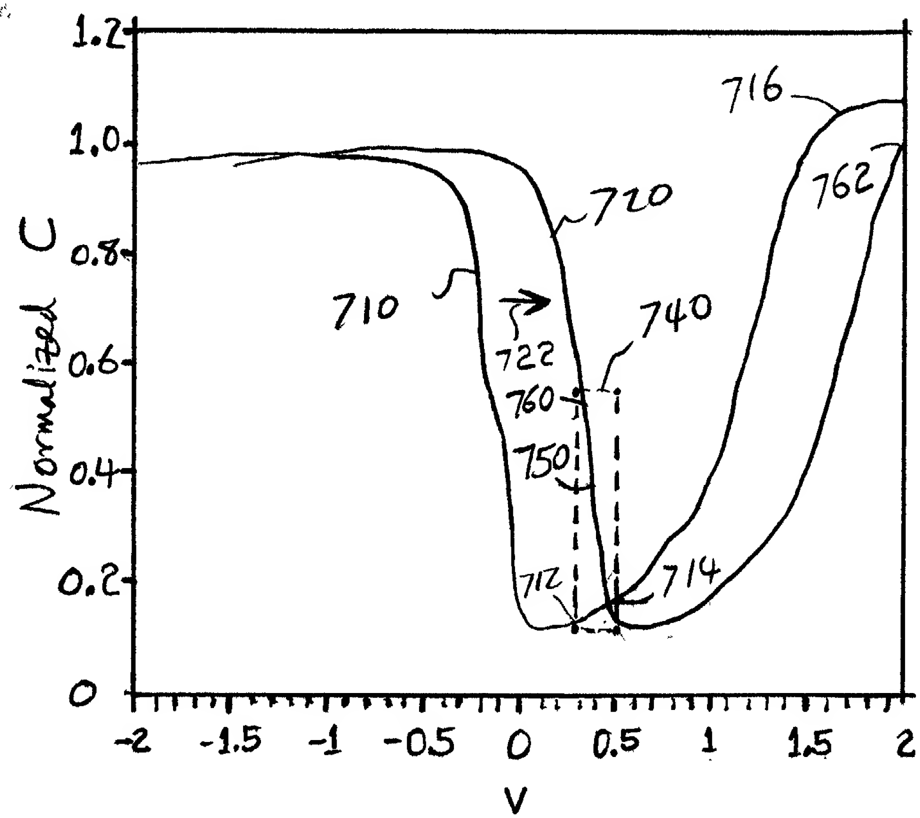


FIG. 6


1.2
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Normalized C
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762

FIG. 7

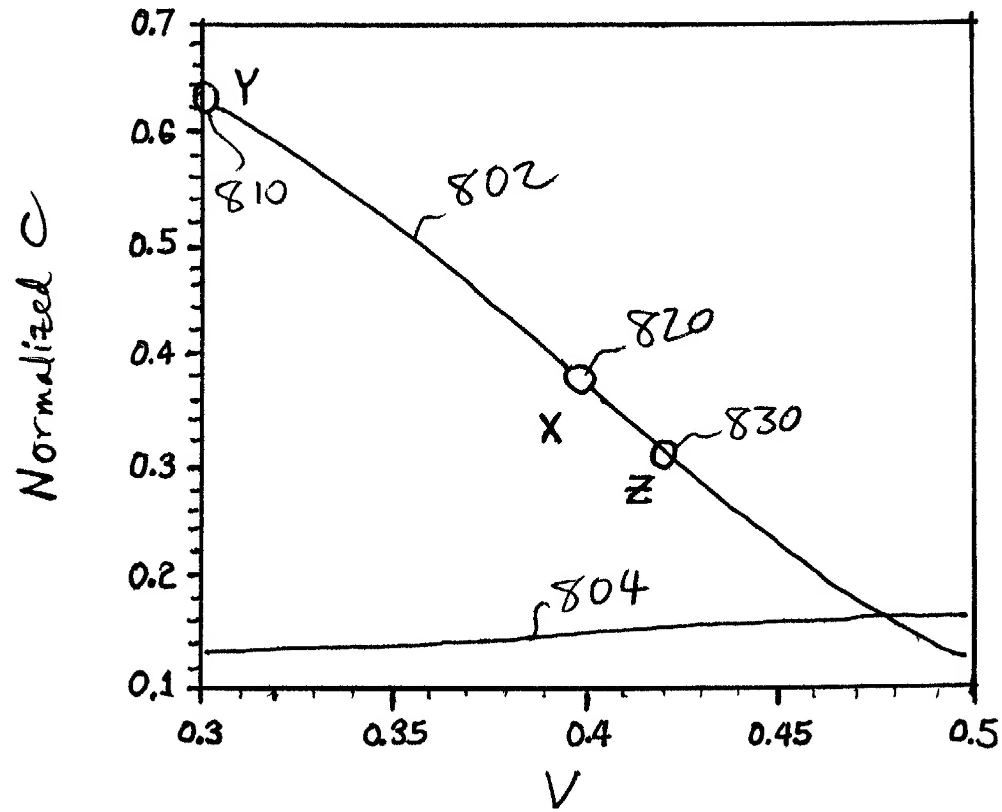
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.3
0.35
0.4
0.45
0.5
Normalized C
V
Y
810
802
820
X
830
Z
804

FIG.8

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR WEAK INVERSION MODE MOS DECOUPLING CAPACITOR

the specification of which

X is attached hereto.
___ was filed on ________________ as
United States Application Number ____________
or PCT International Application Number____________
and was amended on ________________.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Dennis A. Nicholls, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Dennis A. Nicholls, (408) 720-8300.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.